What is claimed is:

1. A method for fabricating a transistor with a polymetal gate electrode structure, comprising the steps of:

forming a gate insulation layer on a substrate;

forming a patterned gate stack structure on the gate insulation layer, wherein the patterned stack structure includes a polysilicon layer as a bottom layer and a metal layer as an upper layer;

forming a silicon oxide-based capping layer along a profile containing the patterned gate stack structure and on the gate insulation layer at a predetermined temperature that prevents oxidation of the metal layer; and

performing a gate re-oxidation process.

2. The method as recited in claim 1, wherein the gate stack structure further includes a diffusion barrier layer in between the polysilicon layer and the metal layer.

3. The method as recited in claim 1, wherein the capping layer is made of one of material selected from a group consisting of $SiO_2$, $SiO_xF_y$ and $SiO_xN_y$.

4. The method as recited in claim 1, wherein silicon oxide-based the capping layer is formed by performing one of an atomic layer deposition (ALD) technique and a plasma

enhanced chemical vapor deposition (PECVD) technique at a temperature in a range from about 70 °C to about 400 °C.

5. The method as recited in claim 4, wherein the step of forming the silicon oxide-based capping layer through the use of the ALD technique includes the steps of:

loading a wafer containing the patterned gate stack structure into a chamber;

flowing a source gas of silicon (Si) into the chamber and purging the remaining gas; and

flowing a source gas of oxygen into the chamber and purging the remaining gas.

6. The method as recited in claim 5, wherein the silicon source gas is one of silicon hexachloride ($SiCl_6$) or silicon tetrachloride ($SiCl_4$).

7. The method as recited in claim 5, wherein the oxygen source gas is a gas selected from a group consisting of $H_2O$, $O_2$, NO and $N_2O$ and a gas obtained by mixing the listed gases.

8. The method as recited in claim 6, wherein the Si source gas is flowed into the chamber as simultaneous as one of pyridine ($C_5H_5N$) or ammonium ($NH_3$) gas functioning as a catalyst for lowering a process temperature is flowed thereinto.

9. The method as recited in claim 7, wherein the oxygen source is flowed into the chamber as simultaneous as one of pyridine ($C_5H_5N$) or ammonium ($NH_3$) gas functioning as a catalyst for lowering a process temperature is flowed thereinto.

10. The method as recited in claim 1, wherein the metal layer is made of one material selected from a group consisting of tungsten (W), molybdenum (Mo), tantalum (Ta), titanium (Ti), ruthenium (Ru), iridium (Ir) and platinum (Pt).

11. The method as recited in claim 2, wherein the diffusion barrier layer is formed with a material selected from a group consisting of $WN_x$, $SiN_x$, $TiAl_xN_y$, $HfN_x$, $ZrN_x$, $TaN_x$, $TiN_x$, $AlN_x$, $TaSi_xN_y$, $TiAl_xN_y$.

12. The method as recited in claim 1, wherein the gate stack structure is formed by stacking a tungsten layer, a tungsten nitride layer and a polysilicon layer.

13. A method for fabricating a semiconductor device with a polymetal gate electrode structure, comprising the steps of:

forming a gate oxide layer on a substrate;

forming a gate stack structure by sequentially stacking and subsequently etching a polysilicon layer, a

diffusion barrier layer, a tungsten layer and a hard mask insulation layer on the gate oxide layer;

forming a silicon oxide layer on a surface of the gate oxide layer exposed by the etching and along a profile containing the gate stack structure by performing an ALD technique at a predetermined temperature that prevents oxidation of the metal layer; and

performing a gate re-oxidation process.

14. The method as recited in claim 13, wherein the silicon oxide layer has a thickness ranging from about 50 Å to about 200 Å.

15. The method as recited in claim 13, wherein the silicon oxide layer is formed by using the ALD technique performed at a temperature ranging from about 70 °C to about 400 °C.

16. The method as recited in claim 13, further comprising the step of carrying out a thermal treatment for densifying the silicon oxide layer and removing impurities contained in the silicon oxide layer after the step of forming the silicon oxide layer.